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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,350	11/25/2003	Jagrut V. Patel	030217	4737

7590 03/22/2006

QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, CA 92121-1714

EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,350	PATEL ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/18/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 5/18/2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 10, 12-14, 21, 23, 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Bodas et al (US Application Publication No. 2004/0003194).

For claim 1, Bodas et al teach the following limitations:

An electronic device (Fig 3), **comprising:**

an electronic component (340 and 341);

and an integrated circuit (320 and 330) **configured to generate a system clock** ("clk in" in Fig 2a) **and an external clock** ("clk out" in Fig 2a) **having a programmable delay from the system clock** (lines 8-11 of [0019] mention that logic 200 and 250 is used together to provide flexibility in controlling the degree of shifting of the clock signal. Thus, the degree of shifting is flexible. In other words, the delay by which the clock shifts is programmable), **the integrated circuit being further configured to provide the external clock to the electronic component to support communications therewith, communicate with the electronic component** (lines 8-22 of [0024] of page 3 mention that 330 generates the clock and shifts the transition of memory clock and memory device use the clock to time the latching of other signals generated by memory controller), **and calibrate the external clock delay as a function of the communications** (lines 24-29 of [0016] of page 2; [0019] of page 2).

For claim 2, 219 is a MUX that chooses the proper delay based on the register 213. Thus, there is a plurality of transmission comprising different external clock delay.

For claim 3, 340 and 341 is a memory.

For claim 10, memory is a SDRAM ([0017] of page 2).

Claims 12, 13, 14, 21 recite the method corresponding to the system recited in claims 1-3 and 10. Since the system recited in claim 12-14 and 21 is configured to perform the

method recited in claims 1-3 and 10, the cited prior art that teaches the limitations of claims 1-3 and 10 also teaches claims 12-14 and 21.

Claim 23 recites the means necessary for the system recited in claim 1 and claim 25 recites the media embodying a program to perform the corresponding method of the system recited in claim 1. The means and media is required to implement the corresponding system and method. Thus, the cited prior art that teaches the limitations of claim 1 also teaches claims 23 and 25.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 5, 6, 11,15-17, 22, 24, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bodas et al (US Application Publication No. 2004/0003194).

For claim 4, the system of Patel et al uses a memory bus to perform varieties of bus activities (lines 9-12 of [0017] of page 2). Thus, the clock having programmable delay is used to sample data read from memory. However Patel et al do not mention about the feedback clock.

The system of Patel et al programs the delay based on route length of clock (lines 24-29 of [0016] of page 2), fine tuning of the timing of a memory bus. In such case, the clock delay setting required to read/write data from memory would be different from the clock delay setting required to sample read data in the controller. Thus, the clock with different delay setting would be needed to sample the read data. That clock can be thought as the feedback clock.

For claim 5, the clock that samples memory read data must maintain the timing requirements. Hence, the clock delay should be a function of communications.

For claim 6, Bodas et al teaches plurality of read/write operations. The delay is different since delay is programmable by software as mentioned in [0025] of page 3. The programming of delay is to ensure safe read/write as mentioned in [0018] of page 2.

For claim 11, Bodas et al do not teach any wireless telephone. However, Examiner takes an official notice that wireless telephone is well known in the art.

One ordinary skill in the art would have been motivated to incorporate the teachings of Bodas et al into an wireless telephone system, since the system of Bodas et al ensures the correct timing of memory in the digital electronic systems. Wireless telephone is digital electronic system that requires memory to store the information. Thus, the

invention of Bodas et al would be beneficial to the wireless system in maintaining the precision of timing of memory.

Claims 15-17, 22 recite the method corresponding to the system recited in claims 4-6 and 11. Since the system recited in claim 15-17 and 22 is configured to perform the method recited in claims 4-6 and 11, the cited prior art that teaches the limitations of claims 4-6 and 11 also teaches claims 15-17 and 22.

For claims 24 and 26, the system of Bodas et al do not explicitly mention about feedback clock. Bodas et al generate delayed clock to read/write data from/to memory. However, the delay depends on route length (lines 24-29 of [0016] of page 2), which is a factor determining the amount of shifting the transition of clock. It is very likely that the delayed clock used to read/write data from/to the memory would be different from the delayed clock used to sample memory read data to the memory controller. The route length to the memory is different from the route length to the memory controller. Thus, the delay used to read/write data from/to memory would be different from the delay used to sample memory read data to the memory controller. The delayed clock that is used to sample data to the memory controller can be thought as the feedback clock of the claimed invention of the pending application.

4. Claim 7, 8, 9, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bodas et al (US Application Publication No. 2004/0003194), in view of Cao et al (US patent Application Publication 2003/0001634).

For claim 7, Bodas et al do not teach that the fixed offset between external and feedback clocks is used to calibrate the delay.

Cao et al teach a system where fixed offset between two clocks is used to calibrate the delay (Fig 3 shows that the two clocks are inputted to 40 and the offset between them is used to calibrate the delay).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Bodas et al and Cao et al. One ordinary skill in the art would have been motivated to calibrate the delay using the offset between two clocks, since that would provide the desired resolution of the delay.

For claim 8, [0029] of Cao et al mention that maximum and minimum delays are stored and used to select a delay to calibrate the new delay.

For claim 9, selecting the center value between lowest and highest delay is within the scope of ordinary skill in the art. One ordinary skill in the art would have been motivated

to select the delay to ensure that the chip is not operating outside the range of max and min value.

Claims 18-20 recite the method corresponding to the system recited in claims 7-9. Since the system recited in claim 7-9 is configured to perform the method recited in claims 18-20, the rejections for 7-9 described above are sufficient to reject claims 18-20.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

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